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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];  
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KESSELS, Jozef, L., W.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **ANDREJIC, Ivan** [YU/CH]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **ELEVELD, Koop, J.**; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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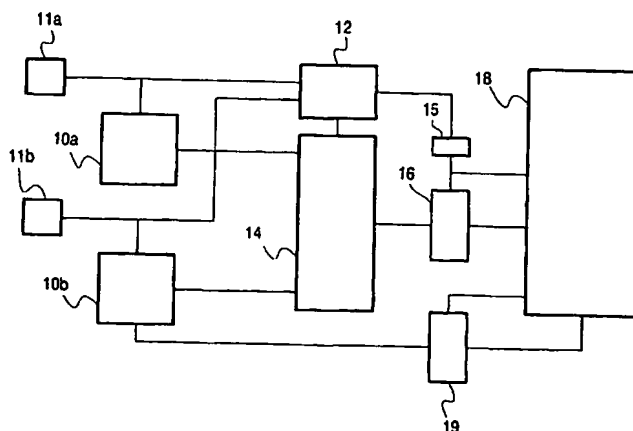
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(54) Title: DATA PROCESSING CIRCUIT WITH MULTIPLEXED MEMORY



(57) Abstract: A data processing apparatus contains several processing circuits each operating under control of its own periodic clock signal, so that the clock signals may have different frequencies and/or can be autonomous. The several processing circuits each have an output for outputting memory access requests, which remain at the output for a validity duration interval defined by the clock signal of the particular processor. A multiplexing circuit multiplexes the access requests to a memory. The memory needs a minimum memory repetition period before it can accept an access request following acceptance of a preceding access request. The clock periods of the processing circuits are longer than the minimum memory repetition period. A timing circuit selects acceptance time points at which each particular access request from a first data processing circuit is accepted. The time point at which the particular request is accepted is always within the validity duration interval in which the particular access request is made. The timing circuit varies the position of the acceptance time points within the validity duration intervals, so that the position is delayed to make room for previously accepting an access request from another processor. The position is subsequently moved back toward a start of the validity duration interval in successive steps during application of successive access requests from the first data processing circuit.

WO 2004/111860 A3



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